WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a MOSFET including a double gate structure provided on the semiconductor substrate; and

an isolation region for isolating the MOSFET from other elements comprising a trench provided on the surface of the semiconductor substrate and an insulator provided in the trench, the isolation region having a region in the trench around the MOSFET, the region having a deeper bottom than other regions in the trench.

2. The semiconductor device according to claim 1, wherein the MOSFET comprises:

a bottom gate electrode provided in the semiconductor substrate;

a top gate electrode provided on the semiconductor substrate above the bottom gate electrode;

a top gate insulating film provided between the top gate electrode and the semiconductor substrate; and

a bottom gate insulating film provided between the semiconductor substrate below the top gate electrode and the bottom gate electrode.

3. The semiconductor device according to claim 1, wherein the MOSFET further comprises a side gate electrode and a side gate insulating film which are provided in the region having the deeper bottom than

the other regions in the trench around the MOSFET, and a part of the insulator is provided in the region having the deeper bottom than the other regions under the side gate electrode.

4. The semiconductor device according to claim 1, wherein the semiconductor substrate is provided with an empty space therein, and the bottom gate electrode and the bottom gate insulating film are provided in the empty space.

5. The semiconductor device according to claim 4, wherein

the trench opens a part of upper wall of the empty space, and the side gate insulating film and the side gate electrode are successively provided on the side of the semiconductor substrate on the empty space opened by the trench.

6. The semiconductor device according to claim 5, wherein the bottom gate insulating film, the side gate insulating film and the top gate insulating film are unified.

7. The semiconductor device according to claim 6, wherein the bottom gate insulating film, the side gate insulating film and the top gate insulating film are formed of a common thermal oxide film.

8. The semiconductor device according to claim 5, wherein the bottom gate electrode, the side gate electrode and the top gate electrodes are unified.

9. The semiconductor device according to claim 6, wherein the bottom gate electrode, the side gate electrode and the top gate electrodes are unified.

10. The semiconductor device according to claim 7, wherein the bottom gate electrode, the side gate electrode and the top gate electrodes are unified.

11. The semiconductor device according to claim 8, wherein the bottom gate electrode, the side gate electrode and the top gate electrodes are formed of a common conductive film.

12. The semiconductor device according to claim 11, wherein the common conductive film is a semiconductor film containing an impurity or film containing metal.

13. The semiconductor device according to claim 4, wherein the empty space remains space which is failed to be filled with the bottom gate electrode and the bottom gate insulation film.

14. The semiconductor device according to claim 4, wherein the empty space comprises an upper wall which includes a flat region.

15. The semiconductor device according to claim 5, further comprises a plurality of empty spaces in claim 4 provided in the semiconductor substrate, the plurality of empty spaces being arranged in a thickness direction of the semiconductor substrate, and a bottom gate insulating film and a bottom gate electrode in

claim 4 are provided in each of the plurality of empty spaces.

16. A method of manufacturing a semiconductor device, comprising:

forming an empty space in a semiconductor substrate;

forming an isolation region on a surface of the semiconductor substrate comprising forming a trench by etching the surface of the semiconductor substrate so that a part of the empty space is opened, and forming an insulator in the trench without closing the empty space; and

forming a MOSFET including a double gate structure isolated from other elements by the isolation region in the semiconductor substrate.

17. The method according to claim 16, wherein the forming the empty space in the semiconductor substrate comprises forming a trench on the surface of the semiconductor substrate, and heating the semiconductor substrate under low pressure.

18. The method according to claim 16, wherein the forming the insulator in the trench without closing the empty space comprises depositing an insulating material on a region including the trench by anisotropic deposition process.

19. The method according to claim 16, wherein the forming the MOSFET comprises forming a gate insulating

film on an upper wall of the empty space and a region including the surface of the semiconductor substrate on the upper wall by oxidizing or nitriding an exposed surface of the semiconductor substrate.

20. The method according to claim 19, wherein the forming the MOSFET comprises forming a conductive film to be processed into a gate electrode by depositing a conductive material on the gate insulating film by CVD process.